# Weekly Report - 04.03.2019

## Analysis of Inductances using Q3D Extractor

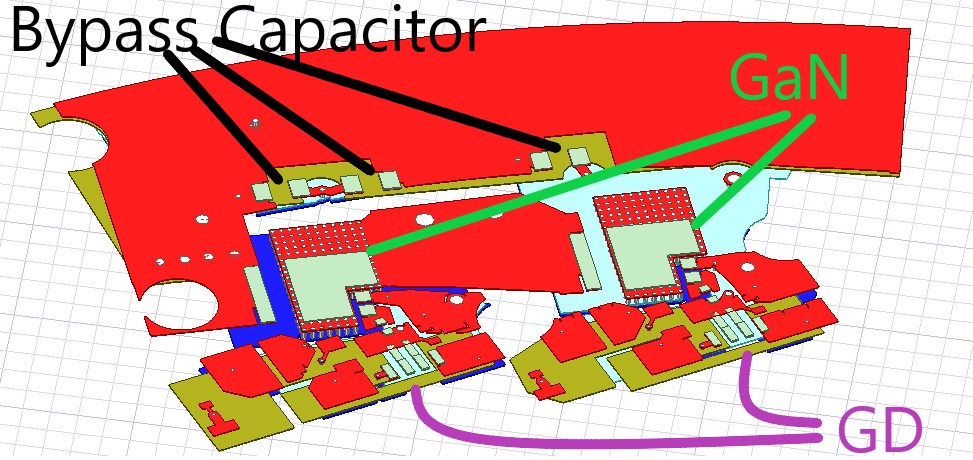


Figure 1: Phase A Layout

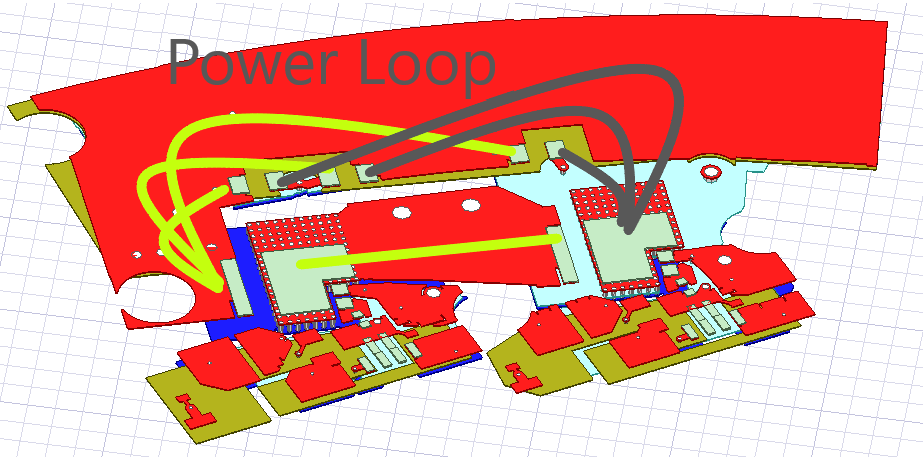


Figure 2: Power Loop

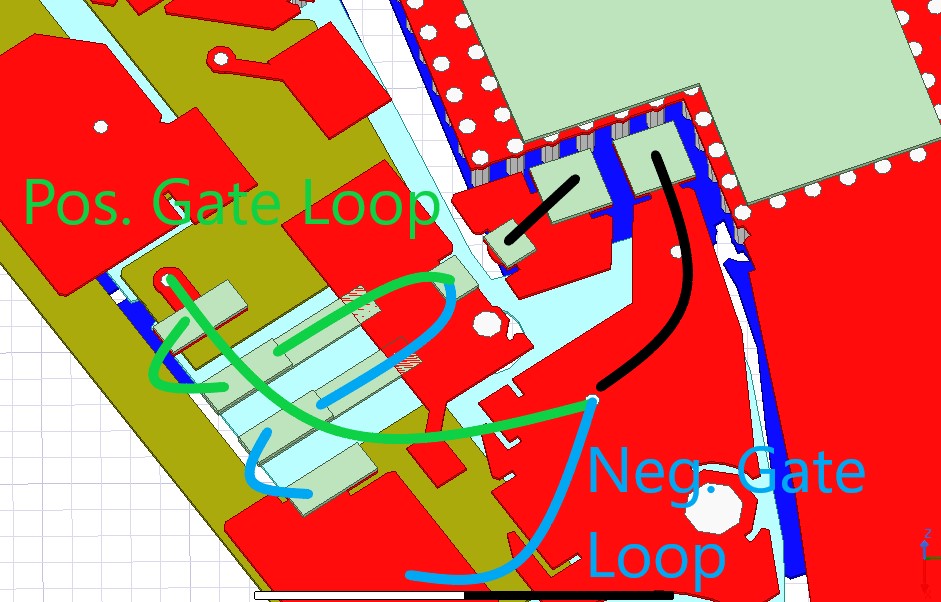


Figure 3: Gate Loops

Table 1: Extracted Inductances

|  |  |
| --- | --- |
| Self Inductances (nH) | |
| Power Loop | 6.28 |
| Top Pos Gate Loop | 6.5 |
| Top Neg Gate Loop | 2.8 |
| Bot Pos Gate Loop | 5.03 |
| Bot Neg Gate Loop | 2.92 |
| Mutual Inductances (nH) | |
| Power – Top Pos Gate | -0.25 |
| Power – Top Neg Gate | -0.205 |
| Power – Bot Pos Gate | -0.106 |
| Power – Bot Neg Gate | 0.0065 |